

1. A method of detecting a reticle option layer in an integrated circuit device comprising:

measuring the current through a first MOS transistor in an integrated circuit device by forcing a test voltage 5 on the drain and the gate wherein said gate and said drain of said first MOS transistor are connected together, wherein the source of said first MOS transistor is connected to a reference voltage, and wherein said first MOS transistor is not parametrically affected by a reticle 10 option layer;

measuring the current through a second MOS transistor in said integrated circuit device by forcing same said test voltage on the drain and the gate wherein said gate and said drain of said second MOS transistor are connected 15 together, wherein the source of said second MOS transistor is connected to a reference voltage, and wherein said second MOS transistor is parametrically affected by said reticle option layer; and

comparing said current through said first MOS 20 transistor and said current through said second MOS transistor to detect the presence of said reticle option layer in said integrated circuit device.

2. The method according to Claim 1 wherein said reticle option layer comprises a threshold voltage implantation.

3. The method according to Claim 1 wherein said reticle option layer comprises one of the group of: polysilicon, metal, and threshold implantation.

4. The method according to Claim 1 wherein said first MOS transistor and said second MOS transistor are the same size, the same direction and in close proximity.

5. The method according to Claim 1 wherein said reticle option layer comprises a combination of reticle layers.

6. The method according to Claim 5 wherein said combination of reticle layers comprises the group of: polysilicon, metal, and threshold implantation.

7. The method according to Claim 1 wherein said measuring of said current through said first MOS transistor and said measuring of said current through said second MOS transistor is by directly probing the die of said integrated circuit device.
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8. The method according to Claim 1 wherein said measuring
of said current through said first MOS transistor and said
measuring of said current through said second MOS
transistor is by probing an output pin of packaged said
5 integrated circuit device.

9. The method according to Claim 1 wherein said first MOS
transistor and said second MOS transistor comprise one of
the group of: NMOS transistors and PMOS transistors.

10. A method of detecting a threshold voltage implantation
reticle option layer in an integrated circuit device
comprising:

measuring the current through a first MOS transistor
5 in an integrated circuit device by forcing a test voltage
on the drain and the gate wherein said gate and said drain
of said first MOS transistor are connected together,
wherein the source of said first MOS transistor is
connected to a reference voltage, and wherein said first
10 MOS transistor has the standard threshold voltage
implantation but not the threshold voltage implantation
reticle option layer;

measuring the current through a second MOS transistor
in said integrated circuit device by forcing same said test

- 15 voltage on the drain and the gate wherein said gate and
 said drain of said second MOS transistor are connected
 together, wherein the source of said second MOS transistor
 is connected to a reference voltage, and wherein said
 second MOS transistor has both said standard threshold
20 voltage implantation and said threshold voltage
 implantation reticle option layer; and
 comparing said current through said first MOS
 transistor and said current through said second MOS
 transistor to detect the presence of said threshold voltage
25 implantation reticle option layer in said integrated
 circuit device.
11. The method according to Claim 10 wherein said first MOS
 transistor and said second MOS transistor are the same
 size, the same direction and in close proximity.
12. The method according to Claim 10 wherein said measuring
 of said current through said first MOS transistor and said
 measuring of said current through said second MOS
 transistor is by directly probing the die of said
5 integrated circuit device.
13. The method according to Claim 10 wherein said measuring

of said current through said first MOS transistor and said measuring of said current through said second MOS transistor is by probing an output pin of packaged said
5 integrated circuit device.

14. The method according to Claim 10 wherein said first MOS transistor and said second MOS transistor comprise one of the group of: NMOS transistors and PMOS transistors.

15. A method of detecting a threshold voltage implantation reticle option layer in an integrated circuit device comprising:

selecting a first NMOS transistor in an integrated
5 circuit device in a first test mode so that the voltage at the drain and the gate of said first NMOS transistor may be measured at an output pin of said integrated circuit device wherein said gate and said drain of said first NMOS transistor are connected together, wherein the source of
10 said first NMOS transistor is connected to ground, and wherein said first NMOS transistor has the standard threshold voltage implantation but not the threshold voltage implantation reticle option layer;
measuring said voltage at said output pin in said

15 first test mode when an internal standard voltage is
connected to said drain and said gate through a first
internal standard resistance;

selecting a second NMOS transistor in said integrated
circuit device in a second test mode so that the voltage at
20 the drain and the gate of said second NMOS transistor may
be measured at said output pin of said integrated circuit
device wherein said gate and said drain of said second NMOS
transistor are connected together, wherein the source of
said NMOS transistor is connected to ground, and wherein
25 said second NMOS transistor has both said standard
threshold voltage implantation and said threshold voltage
implantation reticle option layer;

measuring said voltage at said output pin in said
second test mode when said internal standard voltage is
30 connected to said drain and said gate through a second
internal standard resistance; and

comparing said voltage at said output pin in said
first test mode with said voltage at said output pin in
said second test mode to detect the presence of said
35 threshold voltage implantation reticle option layer in said
integrated circuit device.

16. The method according to Claim 15 wherein said selecting of said first NMOS transistor is by a multiplex circuit and wherein said selecting of said second NMOS is by a multiplex circuit.

17. The method according to Claim 15 further comprising amplifying said voltage at said drain and said gate of said first NMOS transistor and said second NMOS transistor to thereby generate an amplified drain and gate voltage at 5 said output pin.

18. The method according to Claim 15 wherein said first NMOS transistor and said second NMOS transistor are the same size, the same layout orientation, and in close proximity.

19. The method according to Claim 15 wherein said first internal resistance and said second internal resistance comprise the same resistance value.

20. A method of detecting a threshold voltage implantation reticle option layer in an integrated circuit device comprising:

selecting a first PMOS transistor in an integrated

5 circuit device in a first test mode so that the voltage at
the drain and the gate of said first PMOS transistor may be
measured at an output pin of said integrated circuit device
wherein said gate and said drain of said first NMOS
transistor are connected together, wherein the source of
10 said first PMOS transistor is connected to an internal
standard voltage, and wherein said first PMOS transistor
has the standard threshold voltage implantation but not the
threshold voltage implantation reticle option layer;

 measuring said voltage at said output pin in said
15 first test mode when said drain and said gate are connected
to ground through a first internal standard resistance;

 selecting a second PMOS transistor in said integrated
circuit device in a second test mode so that the voltage at
the drain and the gate of said second PMOS transistor may
20 be measured at said output pin of said integrated circuit
device wherein said gate and said drain of said second PMOS
transistor are connected together, wherein the source of
said PMOS transistor is connected to said internal standard
voltage, and wherein said second PMOS transistor has both
25 said standard threshold voltage implantation and said
threshold voltage implantation reticle option layer;

measuring said voltage at said output pin in said second test mode when said drain and said gate are connected to said ground through a second internal standard
30 resistance; and

comparing said voltage at said output pin in said first test mode with said voltage at said output pin in said second test mode to detect the presence of said threshold voltage implantation reticle option layer in said
35 integrated circuit device.

21. The method according to Claim 20 wherein said selecting of said first PMOS transistor is by a multiplex circuit and wherein said selecting of said second PMOS is by a multiplex circuit.

22. The method according to Claim 20 further comprising amplifying said voltage at said drain and said gate of said first PMOS transistor and said second PMOS transistor to thereby generate an amplified drain and gate voltage at
5 said output pin.

23. The method according to Claim 20 wherein said first PMOS transistor and said second PMOS transistor are the

same size, the same layout orientation, and in close proximity.

24. The method according to Claim 20 wherein said first internal resistance and said second internal resistance comprise the same resistance value.